ABSTRACT

An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a standard cell. The standard cell includes a plurality of logic functions. The ASIC also includes at least one bus coupled to at least a portion of the logic functions and a plurality of internal signals from the plurality of logic functions. Finally, the ASIC includes a field programmable (FP) function coupled to the at least one bus and at least a portion of the plurality of internal signals. The FP function provides access to internal signals for observation and control. An ASIC using a field programmable gate array (FPGA) function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of logic, which expresses a test program, into the FPGA function that manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified. In addition, through this system, internal and/or system (external-to-the-ASIC) conditions can be observed. Furthermore, a sequence of resets to different functional blocks can be executed utilizing a system and method in accordance with the present invention. Finally, through this system the end user of the ASIC could write their own error condition correction FPGA code which would communicate using protocols of the existing system error condition architecture.